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Cross-Connected MLI With Reduce Device Count for High Power Applications

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Abstract

This paper presents an asymmetrical cross-connected multilevel inverter (MLI) configuration with reduced device count (RDC). The proposed topology consists of eight power switches, two DC sources, and four capacitors with self-voltage balancing. The generalized topology is formed by two basic modules connected by two power switches. These topologies operate using DC sources and capacitors having the same or different voltage levels, which can be extended by cascading the modules to attain a higher voltage level suitable for high-power applications. Therefore, the proposed MLI is a good choice for renewable energy applications that require a lower input voltage source magnitude to attain high voltage levels. Matlab/Simulink platform simulates the proposed topology using the level-shifted pulse width modulation (LS-PWM) technique. Further, a laboratory prototype is developed to test and validate the feasibility and effectiveness of the proposed MLI. Finally, comparative analysis in terms of total standing voltage (TSV), power switches, drivers, DC sources, and capacitors, is presented against similar recent topologies.

Keywords: Pulse Width Modulation; Total Harmonic Distortion; Multilevel Inverter; Reduced Device Count;

1. Introduction

MLIs have played a leading role in various applications for high and medium voltage/power ratings. The MLIs usage in large areas are dominated by power electronics devices like electric vehicles, wind turbines, active power filters, grid-connected PV systems, induction motor control etc., because of their ability to synthesize high-voltage outputs [1-5]. MLIs can generate various output voltage levels by incorporating multiple capacitors, power semiconductor switches, DC supplies, and diodes. Technically, MLIs are sound in delivering high efficiency, modularity, low THD, high voltage levels, etc. MLIs are broadly classified into three types: Flying Capacitor (FC), Cascaded H-bridge (CHB), and Neutral Point Clamped (NPC). Cascaded H-bridge (CHB) has gained more interest among researchers out of these technologies as it overcomes the drawback of the other two, i.e., high switching losses, unbalanced DC voltage, and the use of more capacitors. Some recently developed and traditional MLI topologies presented in [6, 7] have been briefly reviewed for this work.

Multiple DC source-based CHBs are more appealing than single DC MLIs as of their higher reliability and modularity. Moreover, asymmetric CHB has less complex control than symmetric configurations and significantly increases voltage levels with reduced device count [8, 9]. On the other hand, the count of isolated DC voltage sources required in CHB is significantly higher. Previously, MLIs were limited by needing more DC sources and semiconductor switches. Over the last few years, extensive research has been conducted on improving MLI configuration in every feasible way. In [10–12], MLIs with switched-DC, switched-diode, and switched-capacitor configurations have been proposed. In [13], asymmetric switched-DCMLI has lesser components than traditional circuitry. The proposed topologies in [14] and [15] are cost-effective and perform better in the switched DC source. Even with a reduced device count, these configurations can provide both negative and positive voltage polarity. Besides that, significantly higher voltage levels can be obtained by connecting multiple fundamental units in series. In the presence of an integrated H-bridge, optimized structures in [16, 17] revealed that 15 levels could be generated using 16 interrupter numbers and 7 DC sources in the basic unit. Voltage levels using different DC sources can be generated by having lower switching stress by modifying the same. [18–20] presented and validated the symmetrical and asymmetrical topologies using various pulse width modulation techniques (PWM). [21–23] investigated switched DC-based topologies that can replace traditional MLIs. Two switches connected by a DC link to generate the required voltage level are proposed in [24]. A negative voltage level was created by incorporating an H-bridge into the initial design. This MLI modification was improved in [25], which added two capacitors to get more levels out of each module.

This paper has the following structure: Section 2 discusses the circuit and the working of the proposed CT-Type-MLI. In addition, this section also provides asymmetric configuration and modes of operation, as well

as module extension with output voltage level generation. Section 3 presents the modulation and control techniques followed by the simulation results for the proposed CT-Type MLI. Hardware implementation and the experimental results are presented in Section 4. The proposed MLI's power loss and efficiency are discussed thoroughly in section 5 followed by the detailed comparative analysis of the recent topologies with the proposed CT-Type topology presented in Section 6. Finally, Section 7 contains the conclusion of the paper.

2. Proposed Basic Topology

2.1 Configuration and Operation

Fig.1 illustrates a schematic diagram of a basic CT-type multilevel inverter. It consists of 1 DC source, 2 capacitors, 2 unidirectional switches, and 1 bidirectional switch. The DC supply's bidirectional switches prevent short circuit currents by facilitating blockage of both current polarities. Moreover, using the proposed MLI DC-Link capacitors inherently achieves self-voltage balance. This module has generated the three-level output voltage. Various arrangements for bi-directional switches have been shown in Fig.2.

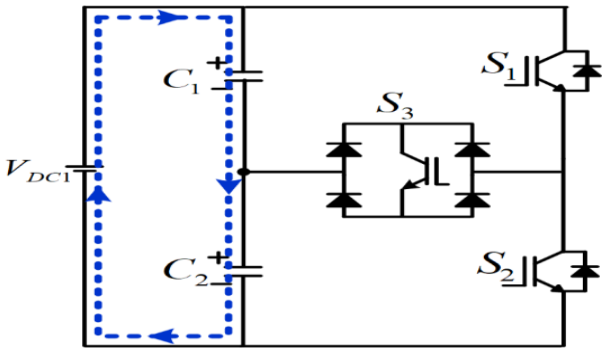


Fig. 1. Basic cell of single-phase CT-type multilevel inverter

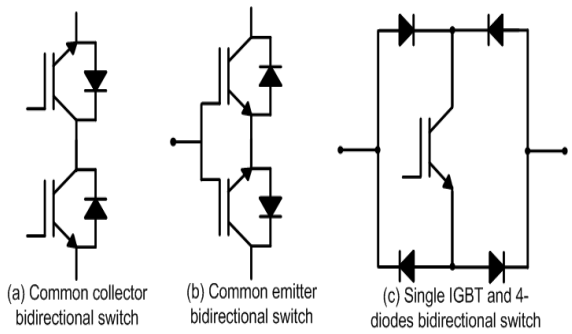


Fig.2: Various arrangements for bidirectional switches

Fig. 3 illustrates the generalized structure of the proposed asymmetric single-phase CT-Type MLI module. A pair of power switches connect the two fundamental modules, L and R. The L module and R module are connected by unidirectional switches S_1 and S_2, and vice versa. Both modules are connected to the load (L and R). This arrangement can produce multiple voltage levels despite having a reduced power device count. Higher voltage levels are expected to significantly lower total harmonic distortion (THD) and low switching frequency.

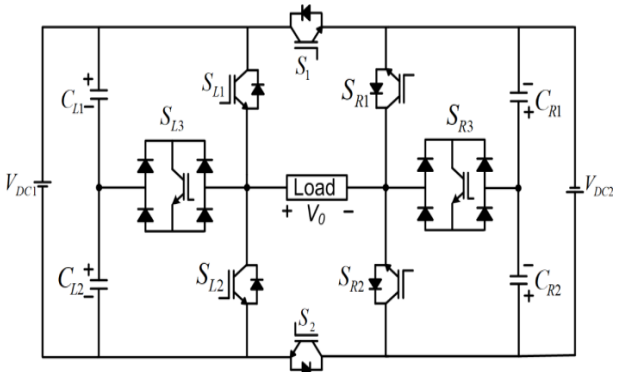


Fig.3: Generalized single-phase CT-Type MLI module

2.2 Voltage stress calculations

TSV of asymmetric operation can be estimated as the switches' maximum voltage standing capacity in the OFF state. The sum of these voltages is used to calculate the TSV of the proposed CT-Type MLI. Table.1 tabulate the TSV calculation for the proposed CT-Type MLI for asymmetrical configuration. Further, the calculation can be expressed as follows:

$$V_{S1} = E + E = 2E,\ V_{S2} = E + E = 2E,\ V_{S3} = 3E + 3E = 6E \quad (1)$$

$$V_{S4} = 3E + 3E = 6E,\ V_{S5} = E + E + 3E + 3E = 8E, \quad (2)$$

$$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} = 36E \quad (3)$$

3. Simulation Study

3.1 Modulation and Control Method of MLI

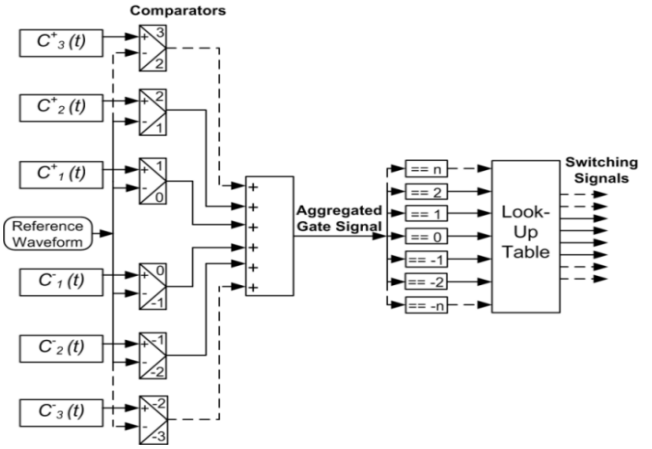
Various modulation techniques are used for MLIs, including high switching frequency techniques (i.e., multi-carrier pulse width modulation and space-vector pulse width modulation) and low switching frequency techniques (i.e., active-harmonic elimination, selective-harmonic elimination and nearest level control). With appropriate modification, the proposed CT-type topology can be modified using any of these techniques. The level-shift pulse width modulation is adopted in this work. The triangular carrier signals are being compared to the sinusoidal reference signal in the LS-PWM technique. Gate pulse generated for switching devices at various voltage levels. The peak value of the waveform is V_{ref},

peak and modulation index (*MI*) will be obtained using eq (4),

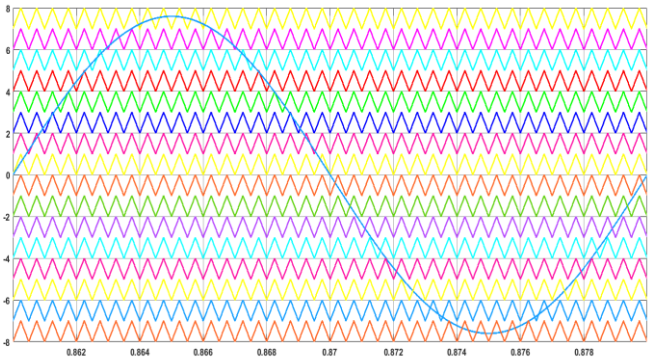
$$MI = \frac{V_{ref.peak}}{5V_{car}} \quad (4)$$

The proposed circuit employs the phase opposition disposition (POD) approach to create gate pulses. Fig. 4(a) shows the schematic diagram of the control technique, and Fig. 4(b) shows the time domain waveform of LS-PWM.

Due to the switching redundancy of particular voltage levels, a specific switching state is chosen to reduce the number of the switching transition of the IGBT device from higher to lower voltage levels. The location of high-frequency carriers decides the PWM signals generated for switches S_1 to S_7.



(a)



(b)

Fig.4: Schematic diagram of (a) control technique (b) LS-PWM waveform

3.2 Simulation Results

MATLAB/Simulink software is used in this sub-section to implement the proposed CT-type MLI with LSPWM modulation. The parameters of simulation are tabulated in Table.1. In the asymmetrical configuration, the input source V_{DC1}= 24V and V_{DC2}= 72 V is applied to get the desired output. Fig. 5 illustrate the 17-level voltage output waveform for the proposed CT-type topology in an asymmetric configuration. The peak value of output voltage is V_{BB} = 96 V at 17 levels of voltage. The proposed CT-type topology load current waveform in an asymmetric configuration is shown in Fig. 6. Fig. 7 illustrates the voltage across capacitors (C_{L1} *and* C_{L2}) in an asymmetric configuration. Similarly, Fig. 8 shows the voltage across capacitors (C_{R1} *and* C_{R2}) in an asymmetric configuration.

Table 3. Simulation Parameters

Parameters	Ratings
Rated DC voltage (Symmetric Configuration)	$V_{DC1} = 24V \; \& V_{DC2} = 24V$
Rated DC voltage (Asymmetric Configuration)	$V_{DC1} = 24V \; \& V_{DC2} = 72V$
Capacitors	$C_1 = C_2 = 2200\mu F$
Modulation index	m_a = 0.85
Load value	L= 20 mH, R=20 Ω
Modulating wave frequency	f_m =50 Hz
Switching frequency	f_s =3150 Hz

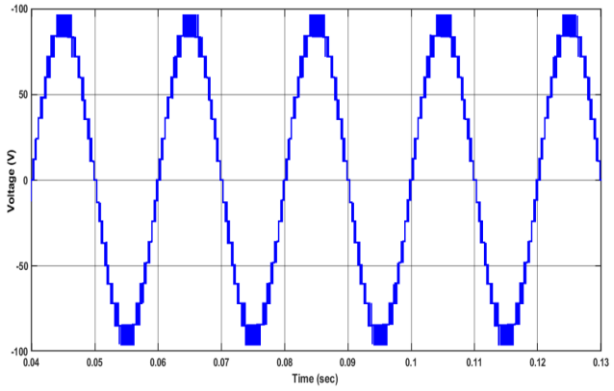


Fig.5. Output voltage of proposed CT-type topology in an asymmetric configuration

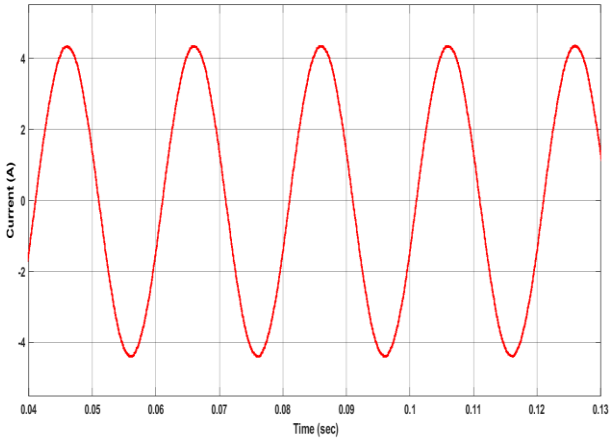


Fig. 6. Load current of proposed CT-type topology in an asymmetric configuration

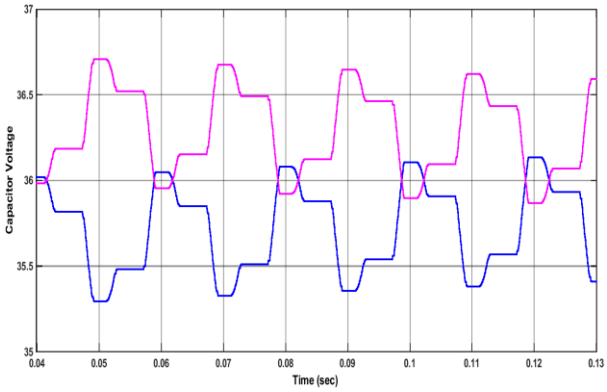


Fig. 7. Voltage across the capacitor (C_{L1} *and* C_{L2}) in an asymmetric configuration

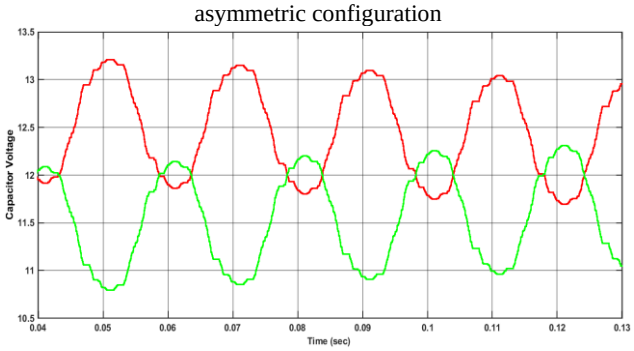


Fig.8. Voltage across the capacitor (C_{R1} *and* C_{R2}) in an asymmetric configuration

4. Conclusion

This paper presents a single-phase CT-Type MLI topology with reduced device count. Also, the operating principles, control design and TSV are explained in detail. The DC-link capacitors achieves self-voltage balance. The main benefit of the proposed work is its capability to generate negative voltage levels without using a modified H-bridge. The proposed topology can be used for high output voltage waveforms without putting additional stress on the power switches. The cascading of modular structures is used to extend the proposed topology for high-voltage levels (17 levels and 289 levels) with a reduced device count. Therefore, this CT-Type MLI is suitable for renewable energy systems and high-voltage/power applications.

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