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High-Speed Low-Power Rail-to-Rail Buffer Amplifier for LCD Flat Panel Display System

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Abstract
High-Speed Low-Power Rail-to-Rail Buffer Amplifier for LCD Flat Panel Display System a low power buffer amplifier for LCD panel driving system is presented. The proposed architecture has self-biased RAIL TO RAIL complementary differential pair for full input output swing, and class B push-pull output driving stage which is suitable for large and small size liquid crystal display, compensation capacitor and resistance are used to improve the settling time and slew rate of the buffer amplifier by stabilizing phase margin, an experimental prototype is simulated using cadence specter in .35 µm CMOS technology which draws only 8 µm static current and provide a settling time of 2.8 µs and rising and 3 µs during four the act area for the design of the buffer is 49*60 µm With power supply of 3.3 it with stand with 1000 pF load capacitance the power consumption of the amplifier under static condition is 66µW.

Keywords: High-Quality, liquid crystal display, low-power, high-speed, high-speed.

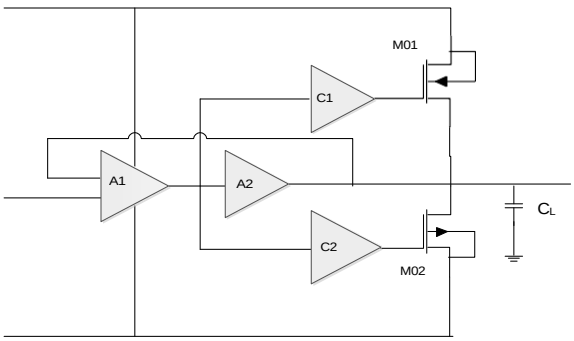
1. Introduction

In order to keep pace with the contemporary evolution of high-quality liquid-crystal exhibits (LCDs), the realization of very compact low-power high-performance output drivers is being given an increasingly elevating accentuation in recent years.
The column drivers of an LCD driving system hold the most consequential role in achieving expeditious speed capabilities, high resolution and low power dissipation, as they distribute the pixel information into the exhibit active matrix. Among the most paramount building blocks of which an LCD column driver is composed, the output buffer amplifiers essentially determine the speed, resolution, voltage swing, slew rate and power consumption of the whole driver [1]
The LCD output buffers are mostly realized by operational transconductance amplifiers in unity-gain configuration, and are typically used to drive the highly capacitive column lines of the exhibit panel. Moreover, as a high open-loop gain is required to obtain a low-valued systematic offset voltage, a two- stage amplifier architecture is traditionally adopted in the LCD driver. Since the adscititious Miller capacitance required for frequency emolument would involve a sensible silicon area consumption, most recently proposed amplifiers achieve stability by exploiting ascendant-pole emolument at the high capacitive- impedance output node. However, to provide high speed driving capabilities to the output stage, a few adscititious current comparators are conventionally included in the rudimentary two-stage amplifier topology, hence requiring some extra.
In this work, we propose a rail-to-rail output buffer with low static-power and high speed for OLED display applications. To guarantee low static power consumption, low tail-current is designed in the buffer's first stage and the output stage is cut off in the static operation. To improve the transient response, dynamic-current-bias technique is used, and it also improves the system stability by pushing
quiescent current from the puissance supply. This work suggests an incipient compact low-power rail- to-rail class-AB buffer amplifier for sizably voluminous-size LCD applications. [2]
The proposed buffer provides a remarkable power efficiency amelioration compared to other antecedently reported solutions. The operation principle of the buffer amplifier along with the foremost design concerns are discussed and analyzed. Simulation results are presented in the last chapter.
The main motivation behind utilizing class-AB buffer amplifier in my thesis work is that this kind of amplifier is having far more preponderant efficiency than class-A amplifier and much lesser distortion than class-B amplifier. It is associated with a biasing network that sanctions the quiescent current to be adjusted, providing an operating point somewhere between class A and class B, hence no supplemental biasing network is required to fine-tune the quandary of quiescent current(leakage current), which ultimately resolved the puissance consumption issues.
Moreover this amplifier is employed with a push-pull output stage. A push-pull output stage is that stage in which pair of active contrivances is utilized that alternately supply current to, or absorb current from, a connected load, and at the output currents from both the transistors is integrated up to instaurate the input signal.

Since this fashion of output is utilized in the buffer, so a very wide range of frequencies could be

covered, withal a very wide range of input could be given to the circuit.
Withal we have utilized rail-to-rail kind of a buffer, hence the replication time of the whole circuit was ameliorated upto a great extent. As a high open-loop gain is required to obtain a low-valued systematic offset voltage, two-stage amplifier architecture is adopted in the LCD driver. However, to provide high speed driving capabilities to the output stage, a few adscititious current comparators are conventionally included in the rudimental two-stage amplifier topology, hence requiring some extra quiescent current from the puissance supply. This work suggests an incipient compact low-power rail-to-rail class-AB buffer amplifier for astronomically immense-size LCD applications.
The implemented buffer provides a remarkable power efficiency amendment compared to other antecedently reported solutions, as both current comparators are liberatingly incorporated into the input differential stage. [1]
The buffer consists of a biasing network, a rail-to-rail stacked-mirror differential amplifier and a push-pull output gain stage. In particular, both output branches of the stacked-mirror amplifier are profitably exploited to realize the two current comparators, which, unlike other antecedently proposed solutions, are therefore implemented without supplemental transistors and power consumption.

Finally, in order to sanction the buffer amplifier to be capable of driving a wide range of load capacitance, phase emolument is performed by introducing a left half-plane zero, which is engendered by the load capacitance CL and the series resistor RC connected between the amplifier output and the load capacitor.
VDD



VIN VOUT
Fig. 1. Block diagram of implemented class-AB buffer amplifier

Liquid crystal display
A liquid crystal exhibit (LCD) is a flat panel exhibit, electronic visual exhibit, or video exhibit that utilizes the light modulating properties of liquid crystals (LCs). LCs do not emit light directly. They are utilized in a wide range of applications, including computer monitors, television, instrument panels, aircraft cockpit exhibits, signage, etc. They are mundane in consumer contrivances such as video players, gaming contrivances, clocks, watches, calculators, and telephones. LCDs have superseded cathode ray tube (CRT) exhibits in most applications. They are available in a wider range of screen sizes than CRT and plasma exhibits, and since they do not utilize phosphors, they cannot suffer image burn-in. A high-speed low-power rail-to-rail buffer amplifier, which is suitable for liquid crystal display driver applications, is proposed. An offset voltage is intentionally built in the second stage to cut off the transistors of last stage from the output node in the stable state and hence achieve low dc power consumption. The input referred offset voltage due to the built-in offset is very small. The buffer draws little current while static but has a large driving capability while transient. An experimental prototype buffer amplifier implemented in a 0.35-μm CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent current of 5 μA is measured. The buffer exhibits the settling time of 1.5 μs for a voltage swing of 0.1 ~ (VDD – 0.1) V under a 600 pF capacitance load. The area of this buffer is 30 × 98 μm2. The measured data show that the proposed output buffer amplifier is very suitable for LCD driver applications.
LCDs are more energy efficient and offer safer disposal than CRTs. Its low electrical power consumption enables it to be utilized in battery- powered electronic equipment. It is an electronically modulated optical contrivance composed of any number of segments filled with liquid crystals and arrayed in front of a light source (backlight) or reflector to engender images in color or monochrome. The most flexible ones utilize an array of diminutive pixels. The earliest revelation leading to the development of LCD technology, the revelation of liquid crystals, dates from 1888. By 2008, worldwide sales of televisions with LCD screens had surpassed the sale of CRT units.
Liquid Crystals (LCs) represent a paradigm studied and exploited in several different contexts. For example, the membrane of a biological cell is composed of lyotropic type LCs which are therefore broadly investigated in the fields of biochemistry, biophysics, and bionics. LCs are additionally studied in the area of pattern- composing mechanisms and in the bifurcation theory, to understand and describe nature structures: snowflakes, honeycomb, and animal coatmarkings are just some examples. They

are preferred to standard isotropic fluids, because they provide more stable and more immensely colossal regions with conventional patterns, and are therefore more facilely overt and controllable (by designates of electric and magnetic fields).
Away the non-dominant pole. Meanwhile, we balance the large-signal slew-rate and system stability with dual-output buffer structure. Placing compensation resistor across the dual outputs creates zero for suitable phase margin, while the real output still behaves with low ON resistance and keeps high slew rate. The proposed design has been verified by a 0.18 μm 1.8 V/5 V CMOS process, which shows that the buffer only draws 2.8-μA static current. Under a 1-nF capacitance load and a 5-V power supply, the buffer achieves 1.18-μs settling time, which is only 41% of the single-output-stage structure with the Flat panel displays require bufers for column driving circuits. These bufers

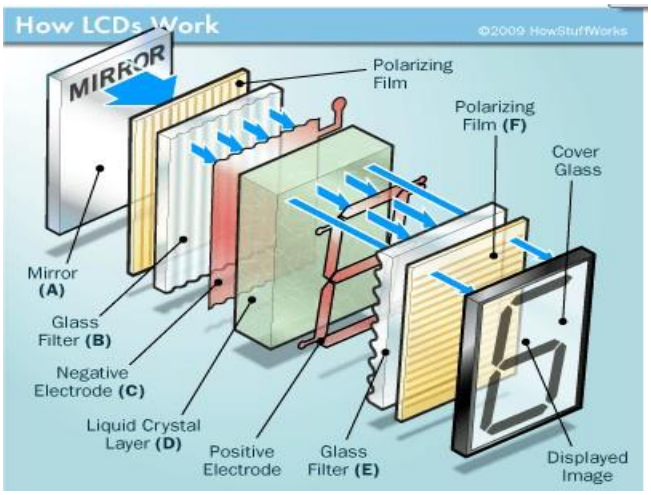


Fig.2.How LCD works

have unity gain and usually drive large capacitive loads. To maintain the railto-rail swing operation, most of the bufer circuits employ complementary diferential pair input stage. Whenever the input voltage is close to supply voltages, one of the driving paths enters the cut-of state. In this paper, a novel adaptive biasing technique for biasing diferential input pair transistors is proposed in order to maintain high driving capacity for the whole input range. In the proposed scheme, whenever an NMOS input stage enters the cut-of stage, the biasing current is boosted for the PMOS input stage and vice versa. As a result, without increasing the biasing current, driving capability of the circuit is boosted in the ranges which are close to the supply voltages. With the proposed biasing scheme, the circuit consumes 45% less biasing current with 16% better settling time as compared to the non-adaptive biased circuit. The proposed biasing circuit and liquid-crystal displays (LCD) bufer is designed using 0.35 [micro]m AMS technology and the SPICE results are reported. The circuit provides high slew-rate and good settling time characteristics which is comparable to the state-of- art LCD driving circuits. Index Terms--Flat panel displays, rail-to-rail bufer, adaptive biasing.
This brief presents the experimental validation of a low-power, large output swing, class-AB buffer amplifier for column drivers of active-matrix flat-panel displays. By exploiting two complementary input amplifiers and a dual-path push–pull output stage, the proposed circuit achieves high-drive performance and rail-to-rail operation. In addition, two current boosters allow area optimization of the output diving transistors by dynamically lowering their threshold voltage. Implemented in a standard triple-well additionally utilized in the field of image processing and analysis. The Liquid Crystal Exhibit is intrinsically a “passive” contrivance; it is a simple light valve. The managing and control of the data to be exhibited is performed by one or more circuits commonly denoted as LCD drivers.[1]

Reflective twisted nematic liquid crystal display.

1. Polarizing filter film with a vertical axis to polarize light as it enters.
2. Glass substrate with ITO electrodes. The shapes of these electrodes will determine the shapes that will appear when the LCD is turned ON. Vertical ridges etched on the surface are smooth.
3. Twisted nematic liquid crystal.
4. Glass substrate with common electrode film (ITO) with horizontal ridges to line up with the horizontal filter.
5. Polarizing filter film with a horizontal axis to block/pass light.
6. Reflective surface to send light back to viewer. (In a backlit LCD, this layer is replaced with a light source.) [14]

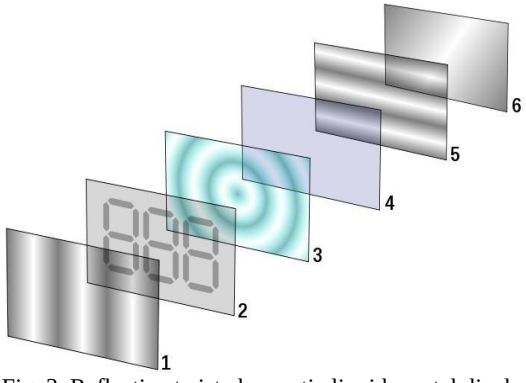


Fig. 3. Reflective twisted nematic liquid crystal display

2. Drivers for AMLCDs

AMLCDs were pristinely conceived for immensely colossal-screen full-kineticism applications, but the injuctive authorization for multimedia handheld equipments with embedded high-quality (minute-screen) exhibits has recently pushed their utilization withal in this market segment.1 Nevertheless, the driver circuits for these two LCD panel categories are subject to different trade-offs:

(1) Minute-area LCDs are typically battery operated and are cost driven and area driven. Thus, the evolution of the driver architecture has been aimed to the reduction of the number of IC components ultimately converging to a monolithic IC (single chip, or combo chip)

(2) Owing to the more preponderant number of rows and columns, immensely colossal-area high- resolution panels cannot be driven by a single chip, which would require an unfeasible number of pins. Besides, sizably voluminous-area LCDs are not stringently fixated on reducing power consumption and dimensions. Their main concern is on performance. Their driver design is hence characterized by a multichip architecture where the main functionalities are implemented by separate specialized ICs.

(3) As already discussed in the antecedent chapter, minuscule-area AMLCDs can be realized either in a- Si and LTPS technologies, whereas astronomically immense-area AMLCDs exploit only a-Si because of the intrinsical wide process variations of LTPS over the substrate area. Research is however performed to surmount this constraint.

(4) Column voltages of minute-area AMLCDs must have a reduced voltage swing (of about 5 V and VCOM-switching is adopted) to employ thin-gate- oxide transistors in the implementation of the Source Drivers, cull driven by size and cost reduction. In contrast, Source Drivers for astronomically immense-size AMLCDs require a higher voltage swing in the range of 16 V, because this fortifies the incrementing number of gray levels required (10 bit per RGB color, at least). Therefore, 20-V thick-gate transistors are adopted. Dot Inversion or column and n-Line inversion is generally utilized in sizably voluminous- area AMLCDs for its more preponderant performance.

3. Results

Simulation and results are obtained using MICROWIND software's. Results illustrate the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 2000pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depicts the simulated transient response to a 50-kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/µs and 14V/µs for the rising and falling edges, respectively, whereas positive and negative settling time values within 90% of the final output voltage are only .6µs and .78µs, respectively.

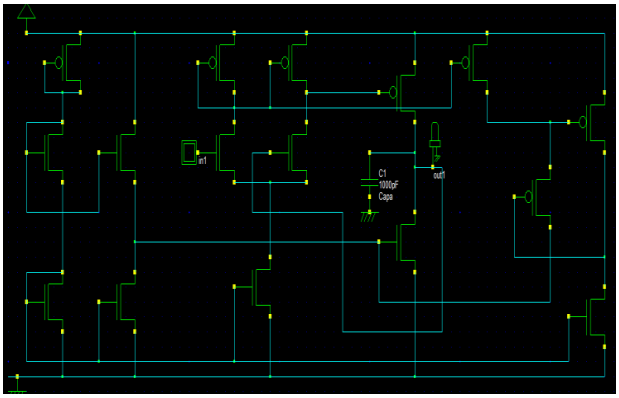


Fig.4. Circuit diagram of the buffer

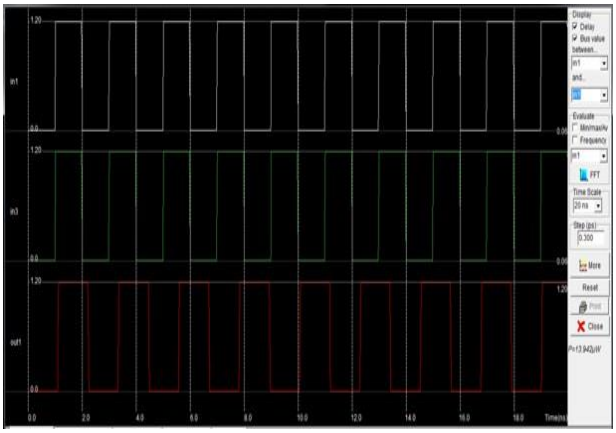


Fig.5. Output waveforms of the voltage at buffer

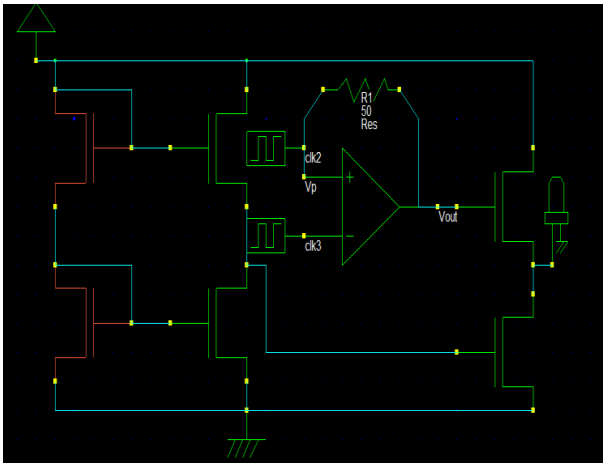


Fig.6. Circuit diagram of opamp buffer

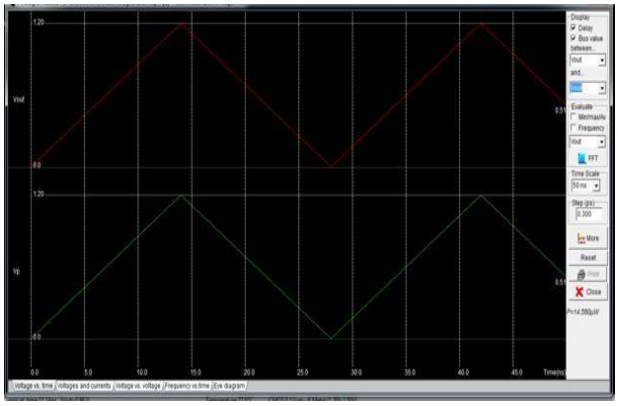


Fig.7. Output waveforms of the voltage at varying load capacitor's value

4. Conclusion

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously.

5. Future Scope

Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilises a only 0.74 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas-

- Since power consumption is low, it has a great future in getting utilized in applications like "ultra low power ADCs".
- Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in "image exhibit contrivances, flat panel exhibits etc.
- Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks .Above are just few examples, but this buffer is having excellent usability in many other areas also.

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