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A Low-Power High-Speed Single Ended CMOS Comparator For Flash Analog to Digital Converter

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Abstract— This paper presents a new low power CMOS comparator for flash analog to digital converter (ADC). The proposed comparator has single-ended type of architecture. The comparator is designed and analyzed by Cadence Virtuoso Analog Design Environment using UMC 180nm technology. Using the proposed comparator, a new low-power 4-bit flash ADC has also been designed and simulated. The proposed comparator consumes peak power of 34.97 µW with propagation delay of 230 ps. The power dissipation of flash ADC is observed to be 500µW only at the speed of 700MS/Sec. The INL & DNL are found to be lesser than 0.6 LSB & 0.1 LSB respectively.

keywords— Inverter, switching voltage, comparator, flash analog to digital converter

I. INTRODUCTION

Comparator constitutes the main component in analog to digital conversion (ADC). It is basically the first stage in ADC, which converts the signal from analog to digital domain. There is variety of comparator design depending upon the application and ADC architecture. The main types of comparator are basically latch comparator, pre-amplifier based comparator and dynamic comparator [1-3].

Typical comparator circuits suffer from the problem of offset voltage and therefore some offset reduction techniques have to be utilized. In conventional type of comparators, pre-amplifier circuit is being employed to lessen the effect of offset voltage [7]. However the author [8] suggested a dynamic latch type comparator, which uses self-calibrating technique for offset cancellation. In this technique, pre-amplifier circuit is replaced by a charge pump circuit. This performs both action of reducing the offset voltage and also minimizing the power consumption of the comparator. However in this method, an additional circuitry is introduced, which makes the design complicated. In the present paper, a simplified design of comparator is proposed. The designed comparator does not use differential type of architecture rather it is based on single ended type. It is primarily designed for flash ADC architecture, which utilizes a bank of comparator. For the N-bit flash ADC, the comparator bank comprises 2^N-1 numbers of comparators. However, these 2^N-1 comparators work simultaneously and therefore consume large amount of power. In addition to this, the flash ADC also requires resistor ladder circuit for reference voltage generation, which is again power starving. In total, flash ADC consumes highest power among all types ADCs. Power dissipation is one of the most important constraints in many low power applications. The designed comparator removes the necessity of ladder circuit as well as preamplifier circuit and consumes very low power as compared to other types of reported comparator circuits.

II. SINGLE ENDED COMPARATOR

An inverter may be deployed as an analog comparator instead of using a whole analog block of comparator [4]. The inverter requires lesser number of transistors as compared to traditional comparator. In fact, a traditional comparator requires two inputs, while inverter based comparator requires only one input. The threshold inverter quantization (TIQ) comparators have been used to design the flash ADC [5]. The variable logic threshold inverter can be scaled to generate a different reference voltages required for comparison. Hence there is no need of resistor array for the generation of reference voltages. Thereby, the static power consumption by resistor ladder is completely removed in Flash ADC. An Inverter can be designed to switching voltages between V_{THN} and $V_{DD} - |V_{THP}|$, where V_{THN} and V_{THP} being the threshold voltages of the NMOS and PMOS transistors respectively. The switching voltage can be expressed as [6]

$$V_{sp} = \frac{(V_{DD} - |V_{THP}|) + V_{THN}\sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}{1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}} \qquad (1)$$

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Where, W_p = PMOS channel width, W_n = NMOS channel width, V_{DD} = supply voltage, μ_n = electron mobility, μ_p = hole mobility. It has been assumed that both transistors PMOS & NMOS have the same channel length. The switching voltage values of Inverters are determined by the relative sizing (W/L) of the transistors.

The threshold voltage of the device is given by the following mathematical expression [6].

$$V_T = V_{TO} + \gamma\left(\sqrt{|(-[2)\phi]_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (2)$$

Wherein, V_{TO} is threshold voltage under zero bias condition V_{SB} is source-to-substrate voltage, ϕ_F is Fermi potential, and the parameter γ is called the body-effect coefficient & described by:

$$\gamma = \left({}^{t_{ox}}/_{\varepsilon_{ox}}\right)\sqrt{2q\varepsilon_{si}N_A} \quad (3)$$

Wherein, t_{ox} is the oxide thickness ε_{ox} is the permittivity of oxide layer; q is the carrier charge, ε_{si} is permittivity of Silicon and N_A is acceptor concentration.

Just by reducing the size of the device and scaling down the supply voltage, the threshold voltage of MOSFETs does not vary. It is clear from the Equation 2 & 3, that threshold voltage is not dependant on the aspects ration (W/L) rather it is a function of MOSFETs oxide thickness. On the other hand, the logical threshold voltage of the device can be change by varying the aspects ration of the device (W/L) from the equation 1.

III. Modified Comparator

The architecture of modified single ended CMOS comparator is similar to TIQ Comparator. The comparator circuit consists of four cascaded circuit stages as shown in figure 1.

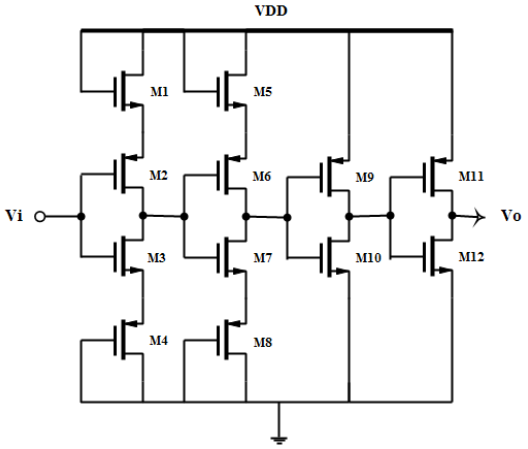

Fig. 1. Proposed Comparator schematics

The first and second stages constitute modified inverters with saturated transistors (M1, M4, M5 and M6) and their logic switching voltage is decided by equation 2. For NMOS device source-drain current (I_D) is described by the following equations.

Note that the devices M1, M4, M5 and M8 are always in saturation because the drain and gate are same potential i.e. $V_G=V_D$. For NMOS device source-drain current (I_D) is described by the following equations.

$$I_D = \frac{W}{L}\left(\frac{\mu_n C_{ox}}{2}\right)(V_{GS} - V_{THN})^2$$

$$I_D = \frac{W}{L}k_n\,(V_{GS} - V_{THN})^2$$

$$gm = \frac{\partial I_D}{\partial V_{gs}} = \sqrt{\frac{W}{L}k_n I_D}$$

Similarly for PMOS device,

$$I_D = \frac{W}{L}\left(\frac{\mu_p C_{ox}}{2}\right)(V_{SG} - V_{THP})^2$$

$$= \frac{W}{L}k_p\,(V_{SG} - V_{THP})^2$$

$$gm = \frac{\partial I_D}{\partial V_{sg}} = \sqrt{\frac{W}{L}k_p I_D}$$

Whrere gm is the transconductance of the device and C_{ox} is the gate oxide capacitance. Note that the devices M1, M4, M5 and M8 are always in saturation because the drain and gate are same potential i.e. $V_G=V_D$. The resistance of saturated MOS Device is given by inverse of its trans-conductance. These resistances are responsible for lower power consumption in the first and second stages. The third and fourth stages are two conventional inverters; their work is just to provide high gain and fast switching.

IV. Flash ADC

The block diagram of 4-bit Flash ADC is shown in the figure 2. An analog input voltage (Vi) goes through each comparator, The comparators compare the input voltage with reference voltages, which are determined by the aspect ratio of CMOS transistor of comparator. The output of the comparator is either '1' or '0' depending on applied input voltage.

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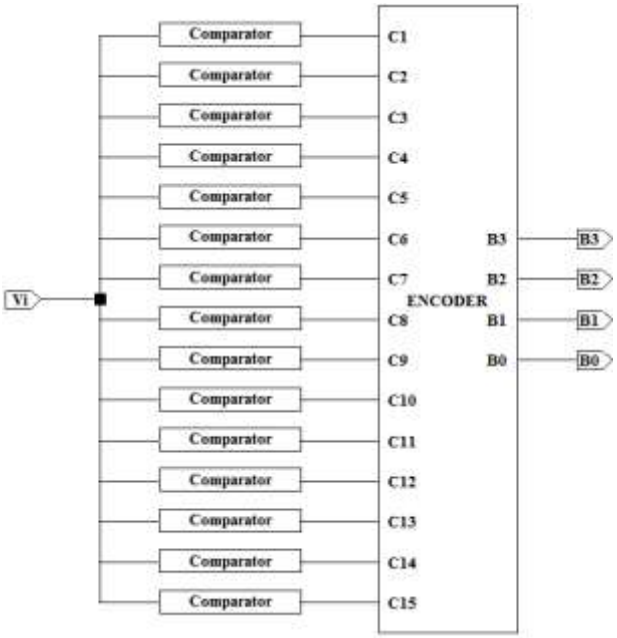

Fig. 2. 4-Bit Flash ADC Architecture

For 4-bit flash ADC, 15 switching voltage levels are the obtained as shown in figure 3. Then comparators output goes to encoder block. The encoder performs the encoding process in two steps. First the comparators output is converted into intermediate code. This code is generated by doing logical EX-OR operation to the two adjacent comparators output.

V. Simulation Results

The proposed Comparator has been simulated at 180nm CMOS process, the supply voltage used is 1.8V. The transient analysis of the comparator is done by giving a ramp input. The voltage transfer characteristic of 15 comparators is shown in figure 4.

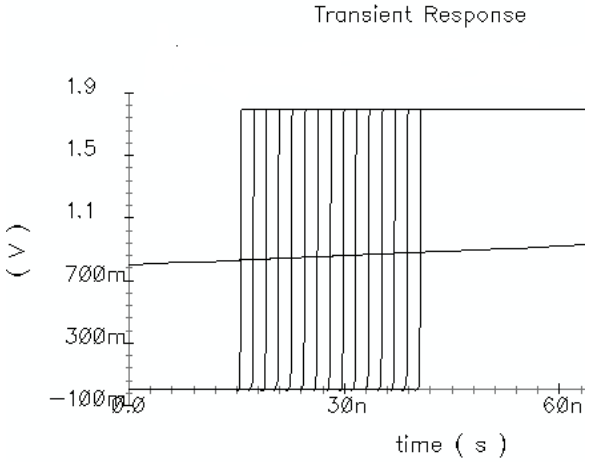

Fig. 3. Variable switching voltage levels for 15 comparators

Using the proposed comparator, a 4-Bit Flash ADC has been designed and simulated at 180nm CMOS process. The design is simpler than the conventional flash ADC and it does not require the resistive ladder for reference voltage generation.
The transient analysis of the ADC is made by giving a ramp input going from 800mV to 920mV and each LSB voltage level is of 3.5mV. The digital codes were obtained correctly for 4-bit ADC as shown in figure 5.

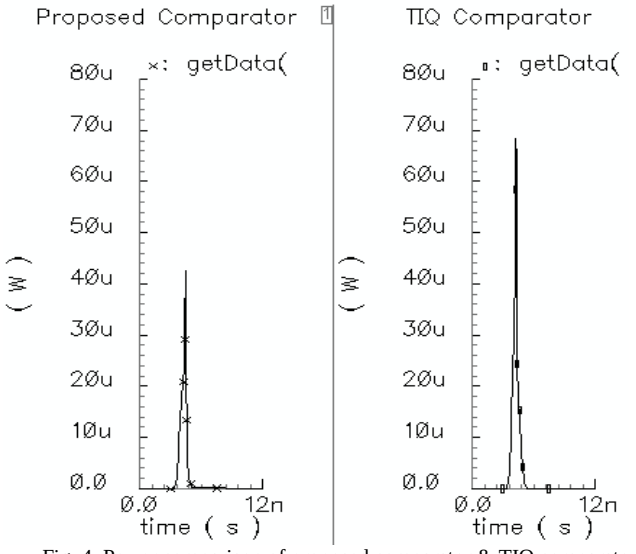

Fig. 4. Power comparison of proposed comparator & TIQ comparator

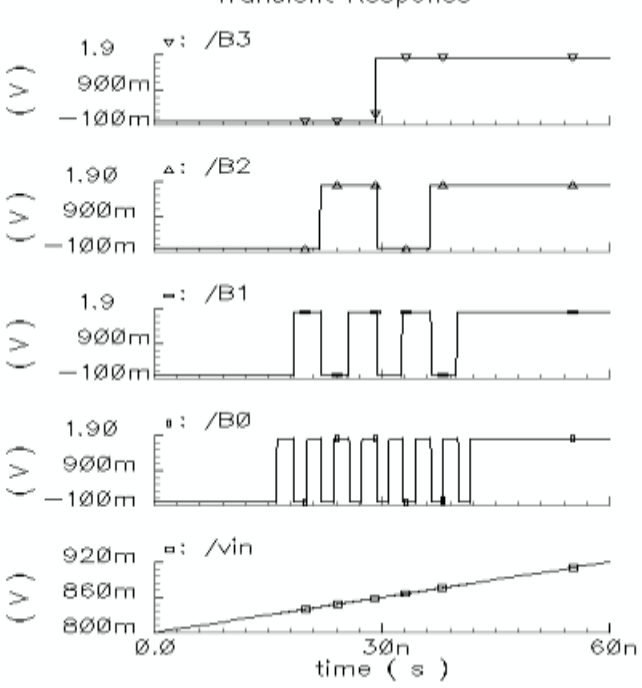

Fig. 5. Transient analysis of the 4-bit flash ADC using proposed Comparator

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VI. DISCUSSION

The different parameters obtained for proposed comparator are compared with TIQ Comparator in Table 1. It has been observed that the peak power for proposed modified comparator is 34.97µW & its average power is only 0.71 µW. While reported comparator [5] consumes peak power of 73.81 µW and its average power is 1.7 µW. There is an almost 47% reduction in the peak power. This is highly desirable for low power application of data conversion circuits.

Table 1: Results Summary

Parameter	TIQ Comparator	Modified Comparator
Peak Power	73.81µW	34.97 µW
Average Power	1.7 µW	0.71 µW
T_{PLH}	166 ps	17 ps
T_{PHL}	517 ps	447 ps
Delay	341.5 ps	230 ps
PDP	25 fJ	8 fJ

The measurement of INL and DNL are shown in the figure 6. It is observed that both INL and DNL are lesser than 1 LSB. This promises a monotonic Flash ADC for reliable conversion of analog signal to digital signal.

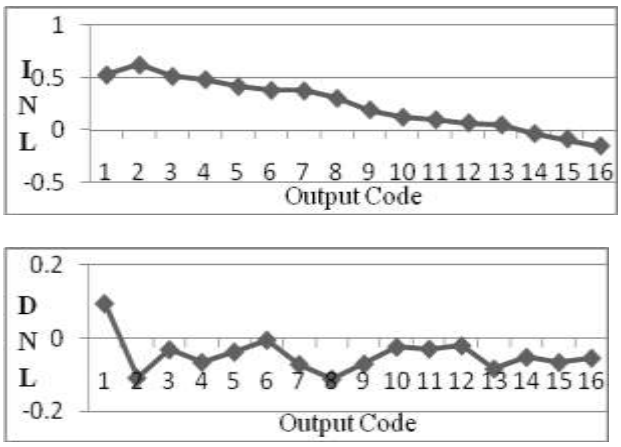

Fig. 6. INL & DNL Measurement

The comparison of performance parameters is carried out with earlier reported work in table 2. For transparent comparison, only flash ADC architectures of 4-bit resolution have been selected. It can be observed from the table that the proposed comparator based ADC consume the lowest power.

Table 2. Comparison of Performance Parameters

Parameters	This Work	[9]	[10]	[11]
Technology	0.18µm	0.18µm	0.18µm	0.18µm
Supply Voltage	1.8 V	1.8 V	1.8 V	1.8 V
Resolution	4 Bit	4 Bit	4 Bit	4 Bit
Speed	700 MS/s	400 MS/s	2 GS/s	4 GS/s
DNL (LSB)	0.1	0.4	-0.04	-0.14
INL (LSB)	0.6	1.1	-0.06	-0.24
Power	0.5 mW	20 mW	42 mW	608 mW
Ladder Network	No	Yes	Yes	Yes

VII. CONCLUSION

The key parameters for the proposed comparator are delay and power dissipation. The proposed comparator dissipates peak power of 34.97 µW with maximum delay of 230 ps. This makes it highly desirable for design of low power, high speed flash analog to digital converter. Using the proposed comparator, 4-bit Flash ADC gives better result in terms of power consumption and speed. The designed ADC achieves speed of 700MS/s with power consumption of 500 µW only. The dynamic parameter INL and DNL are also smaller than 0.6 LSB & 0.1 LSB respectively.

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