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DESIGN OF HIGH SPEED LOW VOLTAGE COMPARATOR DESIGN ON 180nm CMOS

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Abstract

In this paper, A CMOS comparator with high low power application is presented. The comparator has been designed and simulated in 180nm CMOS technology. It is designed to sense low voltage using Double-Tail Dual-Rail Dynamic switching method.

Keywords: ADC,DAC,CMOS,SRAM

Introduction

Comparators are widely used as electronic equipments and as a part of ADC and DAC after operational amplifiers in electronics industries . Comparators are known as single bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. . In the ADC(analog to digital converter) In conversion process, first sampling of the the input signal to be done . This sampled signal is then applied to comparators circuit either in sample and hold circuit or in simple comparator circuit to determine the binary equivalent of the analog signal. The speed of comparator is reduced due to by the delay time of the comparator. Apart from that, comparators may also be used in other applications like zero-crossing detectors, Schmittt trigger oscillator circuit peak detectors, logarithm amplifier ,antilogarithm amplifier, buffer circuit ,voltage to current converter and current to voltage converter circuit and others. The basic function of a CMOS comparator is to find out wheather the test signal is smaller or greater than the reference signal and outputs is a conatant which can be termed as binary signal based on comparison.

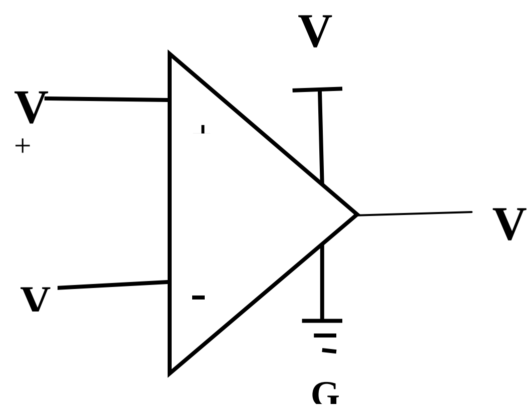

Figure 1 (a): Schematic of Comparator

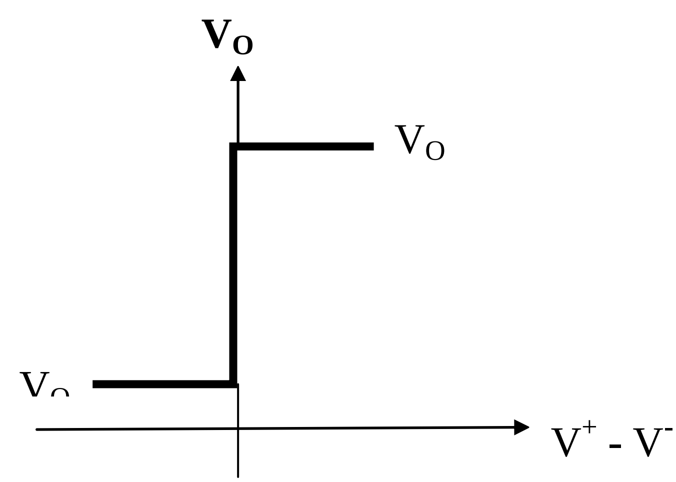

Figure 1 (b): Transfer characteristics of ideal comparator

The schematic symbol and basic operation of a

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voltage comparator are shown in fig1, this comparator can be thought of as a decision making circuit.The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison.

Figure 1(a) shows the symbol of the comparator and 1(b) shows ideal transfer characteristics. V^+ is the input voltage applied to the non inverting terminal input terminal of comparator and V^- is the reference voltage (constant DC voltage) applied to the inverting terminal of comparator. Now if V^+ , the input of the comparator is at a greater potential than the V^-, the reference voltage, then the output of the comparator is a high or logic 1, where as if the V^+ is at a potential less than the V^- , the output of the comparator is a low or logic level 0.

If $V_{INV} > V_{NI}$, then V_o= logic 1 or high.
If $V_{INV} < V_{NI}$, then V_o= logic 0 or low.

Analog signal is a continuous signal of a amplitude values at a given point in time .In a binary signal only one of two given values at any given time, but this concept of a binary signal is too ideal for real-time analysis , there is a transition region between the two binary states. It is important for the comparator to pass the signal without any delay through the transition region of the analog or digital signal. The analysis of comparators will first required characterization of comparators. The comparators is divided into two parts open-loop and closed loop with positive feedback are also called regenerative comparators. The open-loop comparators are basically the comparator in which no compensation is applied . Regenerative comparators are basically non-sinusoidal oscillator uses positive feedback, similar to sense amplifiers used in memory design or simply describe as flip-flops, to accomplish the comparison of two signals. Now a days a third type of comparator which is very popular that is a combination of the open-loop and closed comparators. This combination of comparator results very fast comparator with minimum delays .

COMPARATOR ANALYSIS

1. Comparator based on pre amplification :

Figure 1 shows the comparator based on preamplifier process . The comparator consists of three stages: the input preamplifier stage, a latch stage, and an output buffer stage. The preamplifier stage is basically a CMOS differential amplifier stages. The preamplifier stage amplifies the input signal to improve the sensitivity of comparator sensitivity simultaneously it also cancelled the noise due the regenerative stage . It also reduce input offset voltage. The sizes of M_1 and M_2 are set in such a way that optimum transconductance and minimum input capacitance to be achieved

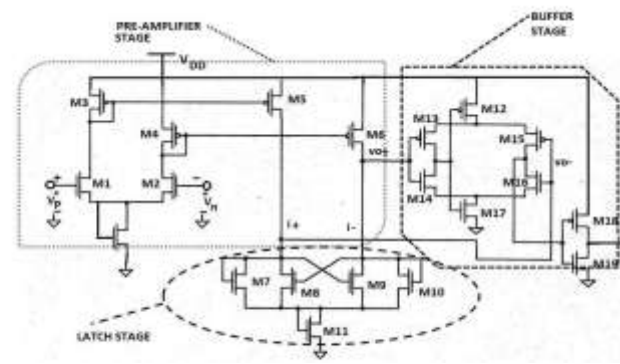

Figure 2: Preamplifier based comparator.

CMOS voltage Sense Amplifier :

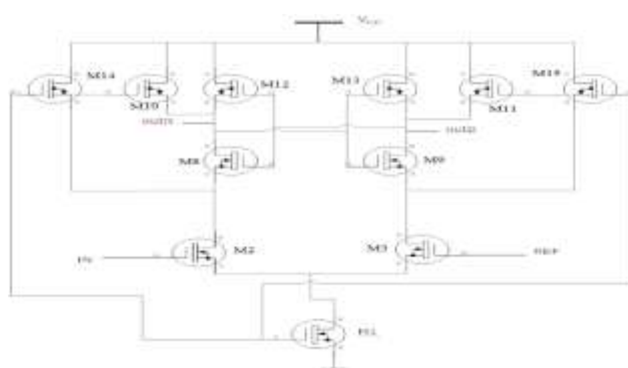

Figure 3: Dynamic Voltage Sense Amplifier .

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Latch type sense amplifiers amplifier is single bit of memory, used in A/D converters, data recei vers and on-chip transistors since they yield their decision making is fast due to regenerativ e feedback. Due to small offset and high speed these are very efficient comparators . Figure 2 shows the circuit diagram of voltage sense amplifier that uses back to back latch stage to pro duce positive feedback. This circuit was first introduced by Kobayashi in 1993 . The current of the differential input transistors M_8 and M_9 controls the latch circuit. A small difference of currents between M_8 and M_9 converts to a large output voltage. Transistors M_{10} and M_{11} are added to increase its speed . These circuits formed single bit flip-flop, used in SRAM.

Voltage SA Double-Tail Latch Type :

Figure3 shows the circuit diagram of the Double-Tail Latch type Voltage SA. Double-Tail comparator uses first tail for input stage and second one is used for latching stage. It operate at lower supply voltages . Large W/L ratio Transistor M_{14} enables to sink large current at latching stage which is independent of common mode voltages at inputs and small size of M_1 offers lower supply voltages resulting lower offset.

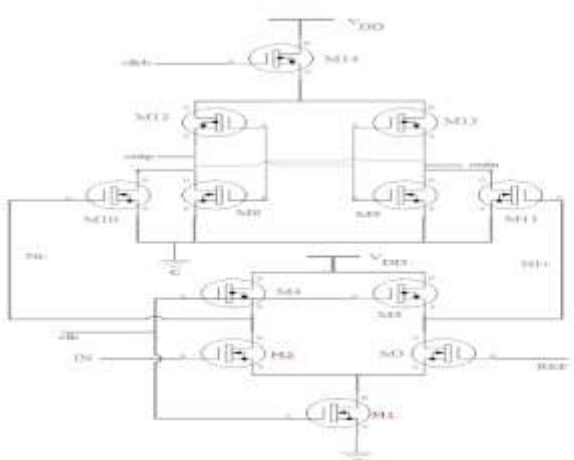

Figure 4: Double-Tail Latch Type Voltage Sense Amplifier

Proposed comparator

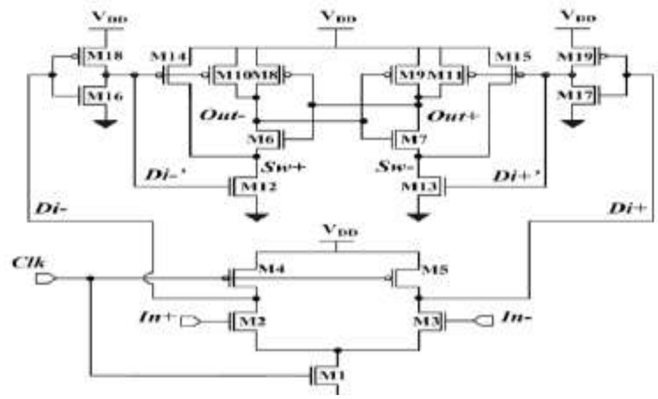

Figure 5. Double-Tail Dual-Rail Dynamic Comparator

Circuit Operation

Reset phase: For its operation, during the pre-charg e (or reset) phase (*Clk=0V*), both PMOS transistor M4 and M5 are turned on and they charge *Di* nodes' capacitance to *VDD*, which turn both NMOS transistor M16 and M17 of the inverter p air on and *Di'* nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 an d M15 are turned on and they make *Out* nodes and *Sw* nodes to be charged to *VDD* while both N MOS transistors M12 and M13 are being off.

Evaluation phase: During the evaluation (deci sion-making) phase (*Clk=VDD*), each *Di* node capacitance is discharged from *VDD* to groun d in a different time rate proportionally to the magnitude of each input voltage. As a result, a n input dependent differential voltage is formed between *Di+* and *Di-* node. Once either *Di+* *or Di-* node voltage drops down below around $VDD-|Vtp|$, the additional inverter pairs M18/ M16 and M19/M17 invert each *Di* node signal into the regenerated (amplified) *Di'* node signal . Then the regenerated and different phased *Di'* node voltages are amplified again and relayed to the output-latch stage by transistor M10−M13. As the regenerated each *Di'* node voltage is rising from *0V* to V_{DD} with a different time interval, transistor M12 and M13 turn on one after another and the final amplification is made between *SW* nodes before the regeneration process. Once either of *SW* node voltages falls below around $VDD-Vtn$, the output latch stage starts to regenerate the small voltage difference at *Out* nodes into a full-scale digital level: *Out+* node will output logic high (V_{DD}) if the voltage difference at *Di'* nodes $\Delta Di'(t)$ is negative $(Di+'(t) < Di-'(t))$ and *Out+* will be low (*0V*) otherwise. Once either of *Out* node voltages drops below around $V_{DD}-|Vtp|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

Simulation Results and Discussion

Circuit Diagram:

Figure 5 shows the schematic diagram of the double tail dual rail comparator This circuit also comprises of latch stage followed by buffer stage.

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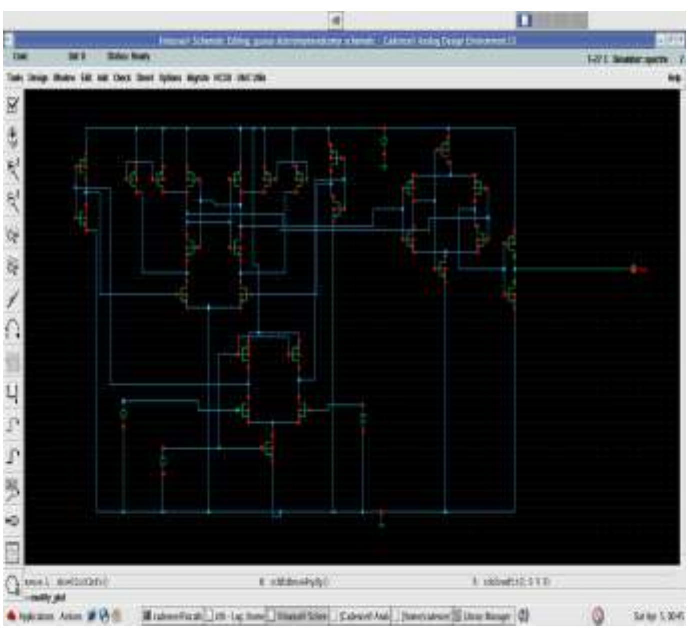

Figure 6 Improved Comparator Circuit

DC Characteristics:

Figure 6 shows the DC response of the circuit. Input voltage is taken as 1 V and swept from -1 .8V to +1.8V. Reference Voltage is taken as 0.7V. From the graph we can conclude that the comparator is working fine.

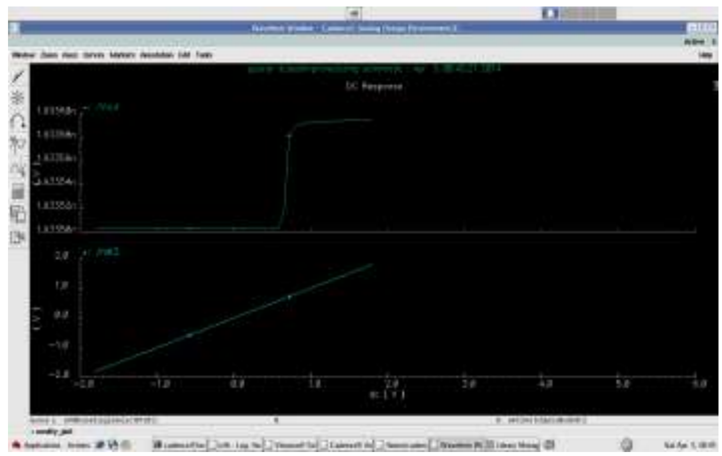

Figure 7 DC Characteristics of the Comparator.

Transient Analysis:

Figure 7 shows the transient analysis of the circuit. From this analysis we can say that the output of *out+* node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

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Figure 8 Transient Response Of Improved Circuit

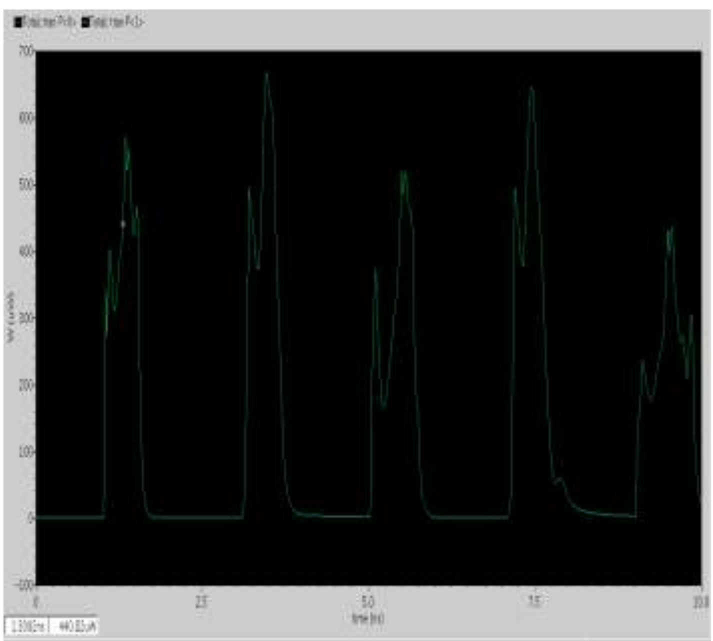

Figure 9 Total Power Dissipation Improved Circuit

COMPARISON TABLE

COMPARATOR	TRANSISTOR COUNT	OFFSET VOLTAGE (mV)	POWER DISSIPATION (μW)	DELAY (nS)	SPEED (GHz)
Preamplifier based Comparator	22	72.8	75.49	2.745	0.364
Latch type voltage sense Amplifier	19	10	26.63	0.415	2.41
Double tail latch type Voltage sense amplifier	22	38	79.01	0.333	3.003
Double tail dual rail Dynamic latched comp (improved circuit)	27	78	102.3	0.293	3.41

CONCLUSION

A new dynamic comparator using positive feedback which shows better response, higher speed, lower power delay product than the conventional pre-amplifier based comparators has been targeted for ADC application. The results are simulated in Cadence® Virtuoso Analog Design Environment with GPDK 180nm technology. In the circuit design, two additional inverters are used in the latched stage. Output of the latch stage in the proposed design is not affected by noise. The transistor count in the proposed comparator is higher to an extent among all the comparators analyzed. After simulation the power dissipation of the comparator is increased by 29.4% and speed is increased by 13.5% as compared to the simulation results that was achieved for conventional double tail comparators.

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