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AN ANALYSIS OF RAIL-TO-RAIL BUFFER AMPLIFIER FOR USAGE OF LCD

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ABSTRACT: Evolution of Low-Power High-Speed Rail-to-Rail Buffer Amplifier for LCD Applications liquid crystal display (LCD) television (TV), there is a large demand for developing high resolution, high color depth driver ICs. The panel of an LCD-TV is larger and higher definition than that of a computer monitor and its color quality requires more accuracy. For example, computer monitors have (262,144) or (16,777,216) colors. However, the LCD-TV needs (1,073,741,824) colors. In order to develop a high-quality display module, the driver system should be promoted to higher color depth and resolution. The evolution of compact, light-weight, low-power, and high-quality displays has caused a large demand for liquid crystal display (LCD) drivers, with features such as low cost, low power dissipation, high speed, and high resolution. An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. Column drivers are especially important for achieving high-speed driving, high resolution, and low power dissipation the realization of very compact low-power high-performance output drivers is being given an increasingly rising emphasis in recent years. The column drivers of an LCD driving system hold the most significant role in achieving fast speed capabilities, high resolution and low power dissipation, as they distribute the pixel information into the display active matrix. Among the most important building blocks of which an LCD column driver is composed, the output buffer amplifiers essentially determine the speed, resolution, voltage swing and power consumption of the whole driver. My thesis addresses a very compact low-power class-B buffer amplifier topology for large-size liquid crystal display applications. The proposed buffer achieves high-speed driving performance, draws a small quiescent current during static operation and offers a rail-to-rail common-mode input range. The circuit provides enhanced slewing capabilities with limited power consumption by exploiting two current comparators embodied in the input stage, which sense the input signal transients to turn on the output stage transistors. A rail-to-rail stacked mirror differential amplifier is used to amplify the input signal difference and supply the bias voltages for the output stage. Post-layout simulations show that the proposed buffer can drive a 1-nF column line load within 1.8s settling time under a full voltage swing, while drawing only 3.5. Monte Carlo results finally confirm an excellent degree of robustness of the proposed topology.

Keywords: *Low-Power, buffer amplifier, rail-to-rail, LCD Applications high resolution, very compact*

1. INTRODUCTION

In order to keep pace with the contemporary evolution of high-quality liquid-crystal exhibits (LCDs), the realization of very compact low-power high-performance output drivers is being given an increasingly elevating accentuation in recent years. The column drivers of an LCD driving system hold the most consequential role in achieving expeditious speed capabilities, high resolution and low power dissipation, as they distribute the pixel information into the exhibit active matrix. Among the most paramount building blocks of which an LCD column driver is composed, the output buffer amplifiers essentially determine the speed, resolution, voltage swing, slew rate and power consumption of the whole driver [1] The LCD output buffers are mostly realized by operational trans conductance amplifiers in unity-gain configuration, and are typically used to drive the highly capacitive

column lines of the exhibit panel. Moreover, as a high open-loop gain is required to obtain a low-valued systematic offset voltage, a two-stage amplifier architecture is traditionally adopted in the LCD driver [1]. Since the adscititious Miller capacitance required for frequency emolument would involve a sensible silicon area consumption, most recently proposed amplifiers achieve stability by exploiting ascendant-pole emolument at the high capacitive- impedance output node. However, to provide high speed driving capabilities to the output stage, a few adscititious current comparators are conventionally included in the rudimentary two-stage amplifier topology, hence requiring some extra quiescent current from the puissance supply. This work suggests an incipient compact low-power rail-to-rail class-AB buffer amplifier for sizably voluminous-size LCD applications. [2] The proposed buffer provides remarkable power efficiency amelioration compared to other antecedently reported solutions.

2. REVIEW OF LITERATURE

Ali Far (2017) A CMOS subthreshold rail-to-rail input-output buffer amplifier suitable for energy harvesting applications is presented, having high gain (AV) of ~ 130dB, consuming ultra low currents (IDD) of ~ 150nA, and operating with low power supply voltage (VDD) > ~ 0.8v. Using a single transistor, the amplifier input stage's tail current is steered between the two PMOSFET input pairs, while one of the PMOSFET pairs is level shifted by a pair of NMOSFET source followers, which keeps the amplifier's input stage transconductance (gm) roughly constant while the inputs span rail-to-rail. Second, to boost folded cascade transconductance amplifier's (FCTA) AV, the proposed plurality of regulated cascode (RGC) current mirrors (CM) utilize a small size auxiliary amplifier, containing the same type and un-scaled FETs as that of the cascoded CMs employed within the FCTA. As such, the boosting of AV is less impeded by the otherwise higher impedance and high capacitance associated with scaled FETs, utilized in most prior art, in the RGC's auxiliary amplifier's signal path. Moreover, the RGC-CM utilizing the same FET, as that of the FCTA's CM, provides more consistency in FCTA's DC, AC, and dynamic response over process and operating condition variations [6].

Sadhana Sharma and Shyam Akashe (2013) A rail-to-rail high speed buffer amplifier is proposed with power gating technique, which is used for flat panel displays. By using power gating technique buffer amplifier has achieved the reduced leakage power by more than two orders of magnitude. The presented buffer amplifier is the combination of two transconductance amplifiers, two current comparators, A push-pull output stage and two sleep transistors. The buffer amplifier is simulated at the 45nm technology with cadence software at 3v supply voltage. The leakage current of this circuit is reduced by 4% (i.e. .79×10-6μA). The settling time for a rail-to-rail buffer swing is settled down to the range of .299×10-6μA [7].

Chih-Wen Lu and Kuo-Jen Hsu (2004) a Large-Swing High-Driving Low Power Class-AB Buffer Amplifier Employing Adaptive-Gain Error Amplifiers -A large-swing, high-driving, low-power, class-AB buffer amplifier, which consists of a high-gain input stage and a unity-gain class-AB output stage, with low variation of quiescent current is proposed. The high-driving capability, low power consumption and low variation of the quiescent output current are achieved by using adaptive-gain error amplifiers whose gains are small in the vicinity of the stable state to reduce the power consumption and the variation of output current, while the high-driving capability is obtained by increasing the gains of the error amplifiers during the transient period [3, 4].

Pang-Cheng Yu and Jiin-Chuan Wu (2018) due to the large number of output buffers on a column driver chip of a flat-panel display, the quiescent current and die area of the output buffer must be minimized. This paper presents a low static power, large output swing, and wide operating voltage range class-B output buffer amplifier for driving the large column line capacitance in flat-panel display. A comparator is used in the negative feedback path to eliminate quiescent current in the output stage [5].

Soo-yang Park et al. (2009) a structural rail-to-rail high voltage CMOS buffer amplifier for driving gamma correction reference voltage of TFT LCD panels is presented. It operates from a single supply and only consumes 0.5mA at 18V power supply voltage. The circuit is designed for 8-bit or 10-bit high-resolution TFT LCD panels. The buffer has high slew rate,

0.5mA static current and 1kohm resistive and capacitive load driving capability. Also, it offers wide supply range, offset voltages below 50mV at 5mA constant output current, and below 2.5mV input referred offset voltage. To achieve wide-swing input and output dynamic range, current mirrored n-channel differential amplifier, p-channel differential amplifier, a class-AB push-pull output stage and an input level detector using hysteresis comparator are applied. The complete circuit is realized in a high voltage 0.18um 18V CMOS process technology for display driver IC and the area measures only 0.056mm^2. The circuit operates at supply voltages from 8V to 18V.

3. PROPOSED APPROACH

The voltages coming from the DAC section must be properly buffered to provide low impedance driving point and current drive capability for the relatively high capacitive source load. R-DACs usually adopt a two-stage operational amplifier in unity gain as voltage buffer. At this purpose, class AB or even B configurations have been exploited to provide sufficient slew rate values, the requirements of the buffers for high-quality display are low power dissipation, large driving capability, small area and large output swing.

In order to keep pace with the contemporary evolution of high-quality liquid-crystal displays (LCDs), the realization of very compact low-power high-performance output drivers is being given an increasingly rising emphasis in recent years. The column drivers of an LCD driving system hold the most significant role in achieving fast speed capabilities, high resolution and low power dissipation, as they distribute the pixel information into the display active matrix. Among the most important building blocks of which an LCD column driver is composed, the output buffer amplifiers essentially determine the speed, resolution, voltage swing and power consumption of the whole driver [1],[8].

There are many challenging design requirements for the output buffers of an LCD driver. Since several column drivers must be used to achieve the required number of outputs, the total number of output drivers should be minimized to reduce system costs and increase reliability; hence, due to the thousands of output buffers which are built in a single chip, each buffer amplifier should occupy a small die area, allowing more output drivers to be integrated on the same chip. Moreover, as each single column driver has more than 720 or 960 output drivers, the static power consumption of the output buffers should be minimized to lower heat generation. Besides, as the display pixels are always updated row by row, the output buffers must be all driven by a step-wise function; consequently, their output voltage should be settled within a horizontal scanning time dictated by the frame frequency and depending on the total number of rows. In addition to the foregoing specifications, an LCD output buffer should also offer an almost rail-to-rail voltage driving which can accommodate a higher number of grey level. The LCD output buffers are mostly realized by operational trans-conductance amplifiers in unity gain configuration, and are typically used to drive the highly capacitive column lines of the display panel. Moreover, as a high open-loop gain is required to obtain a low-valued systematic offset voltage, two-stage amplifier architecture is traditionally adopted in the LCD driver. However, to provide high speed driving capabilities to the output stage, a few additional current comparators are usually included in the basic two-stage amplifier topology, hence requiring some extra quiescent current from the power supply. This work suggests a new compact low-power rail-to-rail class-B buffer amplifier for large-size LCD applications. The proposed buffer provides a remarkable power efficiency improvement compared to other previously reported solutions, as both current comparators are freely incorporated into the input differential stage. [1]

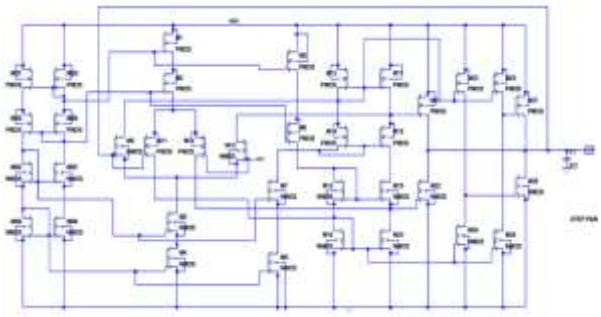

Fig.1 Schematic of proposed buffer amplifier

The transistor-level implementation of the proposed output buffer is illustrated in Fig. 1. As a unitary-gain amplifier, V_{out} is connected to the inverting input Vin-, while the input signal is applied to the non-inverting terminal Vin+. The proposed buffer configuration

contains biasing network (MB1-MB8), complementary MOS differential amplifier, PMOS differential amplifier M1 & M2 for biasing, M11, M12 for differential gain & M16, M20 for active load similarly for NMOS differential amplifier M3 & M4 for biasing, M9, M10 for differential gain & M13, M17 for active load, from M1-M22 altogether constitute complementary differential amplifier working in class AB due to M21 & M22 as shown in fig.2. Both complementary pairs of the input differential amplifier are designed to draw the same current value nIB1/2, whereIB1 is the quiescent current supplied by the bias network devices MB1-MB4 and n is the mirror factor of current sourcesM1 and M4, defined as

$$n = \frac{\left(\frac{W}{L}\right)_{MB1}}{\left(\frac{W}{L}\right)_{M1}} = \frac{\left(\frac{W}{L}\right)_{MB4}}{\left(\frac{W}{L}\right)_{M4}}$$

eq.1

Assuming an equal aspect ratio for transistors M13-M16 and M17-M20, the currents in both branches of the folded-cascode mirror have the same value. Hence, the drain voltages of M14 and M15 are respectively equal to those of M18 and M19. The currents flowing in M14 and M18 are given by

$$I_{M13} = I_{M17} = n\frac{I_{13}}{2} + I_{14}$$

eq. 2

Where IB2 is the drain current of M14 and M18. Since the gate voltages of M21 and M22 are respectively sizing of the current mirror factors of the folded-cascade input stage, and no additional biasing networks are required to maintain an almost constant output current equal to those of M14 and M18, Therefore, the output quiescent current of the amplifier class-AB section can get opportunely set by means of an appropriate, Two current comparators M23, M24 and M25,M26 and a push-pull O/P stage M27&M28, the comparators are used to amplify the voltage difference of the two i/p's, according to the O/P's of the comparator turn ON/OFF the transistor
of the O/P stage. On the other side, to ensure the other driving devices M27 and M28 to stay off during static operation to save in power consumption, the DC drain currents of M23 and M26 are designed to be slightly lower than the nominal drain currents of M24 and M25, respectively. The above specification is fulfilled upon the following design conditions

$$\frac{\left(\frac{W}{L}\right)_{M23}}{\left(\frac{W}{L}\right)_{13}} = \frac{\left(\frac{W}{L}\right)_{M24}}{\left(\frac{W}{L}\right)_{16}} - \Delta\left(\frac{W}{L}\right)$$

$$\frac{\left(\frac{W}{L}\right)_{M26}}{\left(\frac{W}{L}\right)_{16}} = \frac{\left(\frac{W}{L}\right)_{M25}}{\left(\frac{W}{L}\right)_{13}} - \Delta\left(\frac{W}{L}\right)$$

eq.3

implying the gate voltages of M27 and M28 to quickly move towards the highest and lowest supply voltages, respectively, causing both auxiliary devices to be cut off from the output. When $Vin_{(+)}$ decreases the current in M10 & M12 will increase ,but the current in M9 & M11 will decrease, the gate voltage M17 & M16 will increase this will make M23 to be in triode region and that M24 in saturation region, so the drain voltage of M24 will increase and makes M28 to turn ON to discharge the O/P load & M27 is cut-off, until M26 is fully On to discharge. A table1. shows aspects ratio of MOS used in schematic of complementary differential amplifier.

Table 1 shows aspect ratio of MOS used in proposed buffer

Device	Dimension
MB1, MB4, MB5, MB8,M5,M8	5x(1/2.8)
MB2, MB3, MB6, MB7,M6,M7	1x(1/2.8)
M1,M2,M3,M4,M21,M22	10x(1/2.8)
M9,M10,M11,M12	20x(1.5/.6)
M13, M16, M17, M20	(1.2/0.7)
M14,M15, M18, M19	(0.6/0.7)
M22,M26	(0.6/0.6)
M24, M25	(1.8/0.6)
M27, M28	(20/1)

Fig. 2 shows the basic block diagram of the proposed buffer with 2 differential amplifiers cascaded together with 2 comparators and additional transistors used for better power consumption.

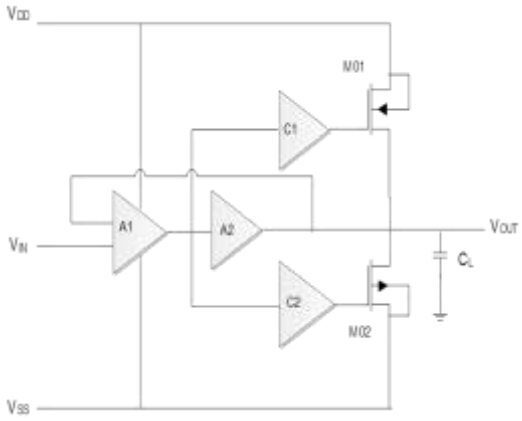

Fig 2 Block diagram of the proposed buffer

This section briefly analyzes the small-signal features of the proposed driving scheme. The simplified equivalent circuit of the proposed output buffer is depicted in Fig. 3, gm1 where and gm2 are the small-signal trans-conductance of the rail-to-rail stacked-mirror differential amplifier and the push-pull output gain stages, respectively, and Ro1, Ro2, and Co1, Co2 are the equivalent output resistances and capacitances, respectively, of the relevant amplifier stages, whereas RC is the compensation resistor and CL is the equivalent capacitance of the LCD panel. In the present analysis, a simple capacitive-load model of the LCD panel is adopted because the worst-case stability condition is considered, since a distributed RC load would help the amplifier stability.[9]

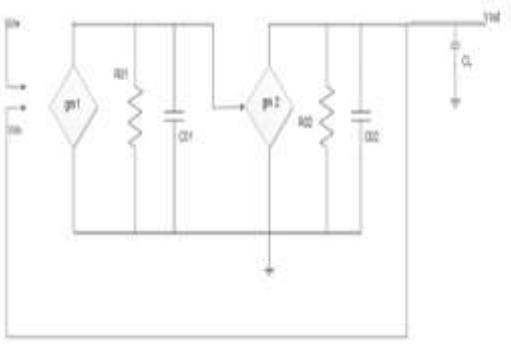

Fig.3 Small signal analysis of the proposed buffer

Assuming Ro1, Ro2 >> RC and Co1, Co2 << CL yields, in the most general case, the following

$$A_V(s) = Ao \frac{(1+\frac{s}{wz})}{(1+\frac{s}{WP_1})(1+\frac{s}{WP_2})(1+\frac{s}{WP_3})}$$

eq4.4

Where Ao is the DC open-loop gain expressed by

$$A_O = g_{m1} \cdot R_{o1} g_{m2} R_{o2}$$ eq4.5

while wP1,wP2 and wP3 are the frequencies of the three amplifier real poles, which are, respectively, given by

$$w_{P1} = \frac{1}{(Ro2 + Rc)C_L} \approx \frac{1}{Ro2C_L}$$

$$w_{P2} = \frac{1}{R_{o1}C_{o1}}$$

$$w_{P3} = \frac{1}{(Ro2 \| Rc)C_{os}} \approx \frac{1}{R_C C_{os}}$$

eq. 6

And wZ is the frequency of the left-half plane zero introduced by the compensation resistor RC, which is given by

$$wz = \frac{1}{R_C(C_L + C02)}$$

eq.7

The equivalent circuit contains three poles. However, the third pole frequency, wP^3 , is far away from the other poles, and its contribution to the amplifier transfer function in (1) is negligible.

The dominant pole of the circuit originates from the high-valued load capacitance, while the second pole frequency is determined by the equivalent resistance and capacitance of the amplifier internal node, and does not depend on the load capacitor.

4. SIMULATION AND RESULTS

Simulation and results are obtained using MICROWIND software's. Results illustrate the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 2000pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depicts the simulated transient response to a 50-

kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/µs and 14V/µs for the rising and falling edges, respectively, whereas positive and negative settling time values within 90% of the final output voltage are only .6µs and .78µs, respectively.. As can be observed, the output waveform follows the input waveform. The major performance parameters of the analyzed buffer are summarized and compared to other conventional topologies in Table 2, which shows a remarkable improvement of the proposed amplifier over other previously reported buffers

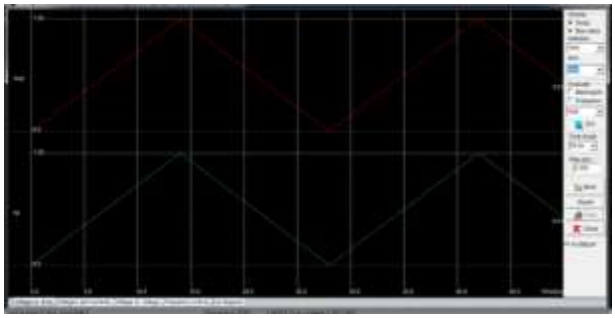

Fig. 7 Output waveforms of the voltage at varying load capacitor's value

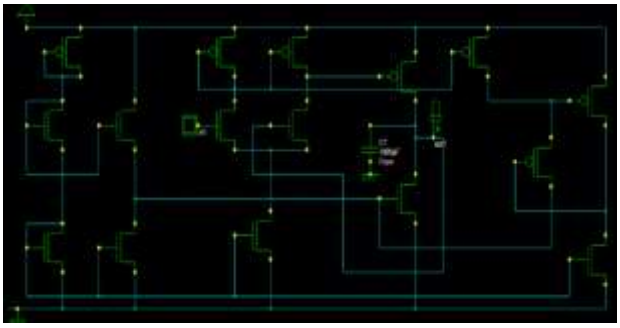

Fig. 4 Circuit diagram of the buffer

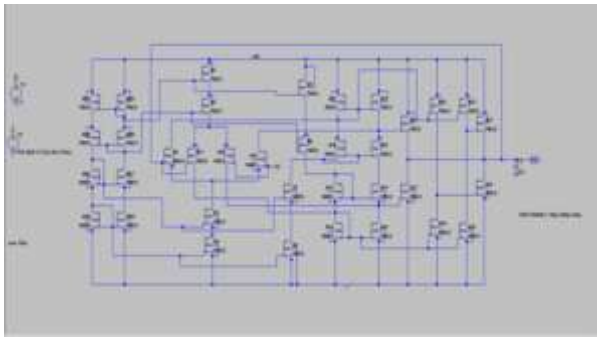

Fig.8 Circuit diagram of the main buffer implemented

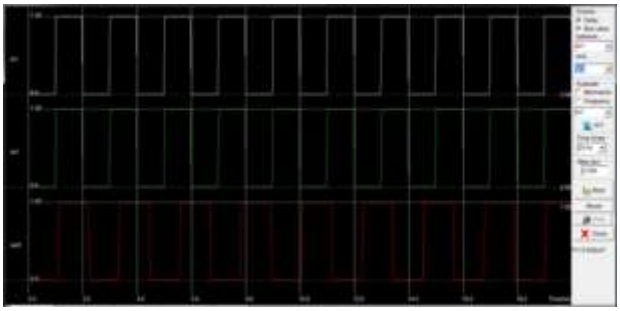

Fig.5 Output waveforms of the voltage at buffer

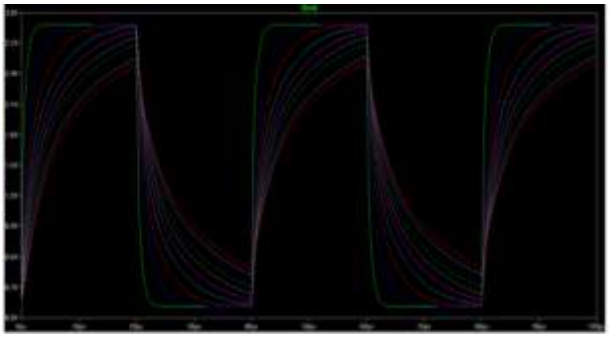

Fig.9 Output waveforms of the voltage at varying load capacitor's value

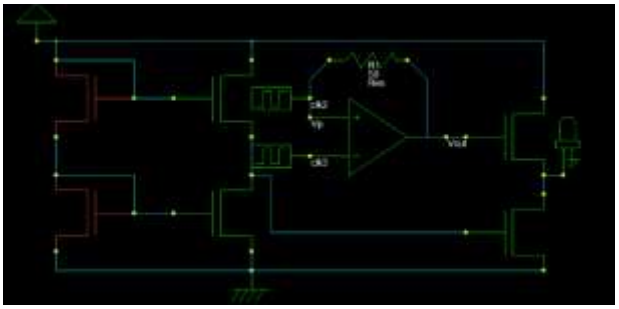

Fig. 6 Circuit diagram of opamp buffer

Table 2 Comparison Table

	Ref.[10]	Ref.[15]	Ref.[17]	Ref.[1]	This work
CMOS TECHNOLOGY	0.8μm	0.35μm	0.35μm	0.6μm	0.6μm
OPERATION CLASS	B	B	AB	B	AB
SUPPLY VOLTAGE (V)	5	3.3	3.3	3	3
LOAD CAPACITOR (pF)	600	600	1000	1000	2000
QUIESCENT CURRENT (μA)	24	7	7.7	3.5	4
SETTLING TIME (μs)	5.5	2.8	1.28	1.7	0.6
IN/OUT RANGE (V)	80%	100%	100%	100%	80%
ACTIVEAREA (μm^2)	230*140	46*58	25*25	30*30	21*27
POWER DISSIPATION (mW)	NA	NA	NA	NA	1.05 mW
SLEW RATE (V/μs)	NA	NA	NA	NA	12V/μs

5. CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence, the high speed self-inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously.

Future Scope

Since the dissertation topic implements a very compact, high-speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilizes an only 0.74 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas:

- Since power consumption is low, it has a great future in getting utilized in applications like “ultra low power ADCs”.
- Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in “image exhibit contrivances, flat panel exhibits etc.
- Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks. Above are just few examples, but this buffer is having excellent usability in many other areas also.

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