Engineering Universe for scientific Research and management
ISSN (Online): 2319-3069
Vol. XIV Issue VI
June 2022

Review on Domino Logic Techniques for High Speed Low-Power Logic Circuit Application

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Abstract

In this paper, the relation of static and different domino designs is reviewed on the basis of different factors for the betterment of modern communication services. Noise immunity, leakage and speed are the three most important factors which is considered, while designing high speed wide fanin logic gates. Improving the noise immunity and reducing the leakage current without affecting the speed for logic gates is a challenging task for the circuit designs. In this work the speed performance of various domino logic circuit designing styles, the design of logic gates has been reviewed by analyzing key parameters such as normalized unity-noise-gain (UNG), power consumption, threshold fluctuations and delay.

Keywords: Domino and static logic, noise reduction, normalized unity noise gain.

1. Introduction

Noise margin is amount of noise that digital Circuit could withstand without compromising the operation. Noise margin does construct that any signal which is true with limited noise included to it, is still recognized as true and not false. It is the difference of signal and noise value.

Very large-scale integration (VLSI) made a possible way for compact circuits with more transistors so that, it improves the performance even so this method makes a criterion in the design of submicron. Noise immunity requires more attention in dynamic spectrum management (DSM). Various leakage currents increase rapidly, which varies clock frequencies.

Greater value of interference and other interference reduces the noise-immunity of different circuits. The reduction of noise-immunity is achieved by reducing the threshold voltage even so it improves the sub-threshold leakage currents, which also improves power. The usage of processors increases in modern electronic devices. Dynamic logic has become the option of circuits as it accomplishes in other ways. There are many sources in domino logic circuits, that they are categorized into two general types; gate-internal interference, which includes charge-sharing interference, leakage interference and external interference. A new method (Transparency window technique) which increases the noise immunity with the precharge of one internal-node of negative logic and separating the precharge-node and the output from the given signals throughout the evaluation phase, is made to improve the noise tolerance of digital circuits. Besides other techniques to improve noise immunity in oscillators, dynamic circuits and CMOS integrated circuits (ICs). Current leakage plays a vital role in designing IC's, device dimension is a particular reason for leakage.

Meanwhile supply and transistor threshold voltages are also reason for the leakage current. Power dissipation is the one of the major factors should be analyzed in digital circuits. Digital CMOS circuit contains various component like dynamic power component, short circuit power component, and static power component. These factors of power component could be reduced and designed. They are transistor sizing, voltage scaling, voltage islands, variable supply of $V_{DD,}$ and multiple threshold.

Transistor sizing changing the size of gate or transistor which plays important role in reduce power component. Voltage scaling is suppling low voltage to the digital circuit but lead to the performance slower. In voltage islands the voltage islands the level shifter is implemented to different supply voltage of circuit. Variable V_{DD} consist of two factor they are high voltage V_{DD} and low voltage V_{DD} where high voltage is applied the circuit speed increases enormously and low voltage V_{DD} is applied thus circuit becomes slower but low voltage V_{DD} is allowable in the circumstance where the slow operation does not affect performance of digital circuit. Multiple threshold is classified in to two they are high voltage threshold and low voltage threshold. High voltage threshold transistor would produce slow operation but it leaks less. Present-day the transistor designed with various different threshold voltage. Power gating is one of the techniques where the power is closed or blocked when the transistor is not switching. Transistor is designed with long channel will lead to leak less power but the transistor circuit becomes larger and performance become slower. There are various methods of reducing power dissipation in circuit level and logic level operation. Power can be analyzed and estimated using SPICE software and other analysis are carries out like static timing analysis, logic simulation. Register and transfer level logic operation analysis lead to high speed and capacity

but analysis of register and transfer level not accurate. The rest of this paper line up as follows. The domino design is reviewed in Section III. Section IV consists of comparison of proposed designs for the domino logic in performances which also reduce the external factors. Section V culminates the result.

2. Static Circuit Design

Static logic design has the ability to make the output high or low of the circuit. It has no minimum clock rates. The clock rates cloud be an ability to pause a system. The static logic design has a great advantage by pausing a system [7]. Thus, it is able to pause any time makes debugging much easier to implement the single stepping. Single stepping gives instruction in terms of a computer program. Single stepping is very compact to determine its functioning where the entire system able to run in low clock rates, which allows the low power consumption to the electronics to run for a long time with the given power supply. Static gates are straightforward to design and it is controllable with high noise immunity. In static design technique where the output is driven because it is connected to either Vcc or the end. The static circuit has an advantage on withstanding in high radiation so this type of design used in space technology [3].

3. Dynamic Circuit Design

Dynamic logic is playing a major role in greater speed applications, where domino logic is based on CMOS domino logic techniques. It was integrated to increase the speed of the circuit [8]. Input of the circuit is provided with a clock and output is connected with inverter. It works twice as fast as the static logic. Generally dynamic logic has two phases for the operations. They are setup phase and evaluation phase, in which the output goes high or reaches the maximum value and also the clock value will be high [7]. Some techniques are proposed in [10]. They are used to find issues in the design.
Such techniques are HSD, CKCCD, CKD and LCR[5], by using evaluation techniques, it is further classified as Diode-Partitioned Domino (DPD) and Diode Footed Domino (DFD)[6].

A. Standard foot less domino

The technology scaling resulted in the scaling down of power consumption and supply voltage, however it also caused increase in sub-threshold leakage current and reduction in prevention of noise. The standard footless domino (SFLD) circuit, a footer transistor is used for wide in OR gates and it uses a footless domino gate [1]. The footless topology is utilized to obtain high-performance design. This method involves a comparatively compact keeper transistor, but the prevention of leakage is increased by using a footer transistor in diode arrangement. This technique also uses a current mirror method to make better performance in the evaluation network. The domino circuit is changed by connecting an NMOS transistor in diode arrangement in cascade with the evaluation network. The reduction of sub threshold leakage is achieved using the diode footer transistor by an occurrence called the stacking effect. At evaluation network voltage drop occurs due to the leakage of evaluation transistors, which helps to exponentially reduce the sub threshold network. The diode footer also provides higher gate switching voltage which leads to increased noise immunity but also results in performance degradations due to reduction in evaluation current. Thus, another mirror transistor is used for mirroring the evaluation current from precharge node. Thus, the standard footless domino (SFLD) circuit uses the diode footed technique to achieve high performance, leakage tolerant, low sub threshold voltage, low power consumption and high noise immunity circuit [10].

B. Conditional keeper domino

In rapid timing plans, the input signals are prepared before (or) close to the beginning of the dynamic gates. The output of the dynamic gates is shown to the leakage and distortion for an unnecessarily for more time [2]. The entire operating time is used to cover the sized-up the standard keeper in conventional dynamic circuits. The performance of the gate will be degraded since the standard keeper starting of the evaluation phase executing unconditionally, variable strength is possessed by conditional keeper circuit. Throughout the process transition at output of keeper is weak and hefty during the evaluation. The dynamic output should be high. At one stage of the evaluation phase, the clock signal turns to false to true. Logic gate plays a major role for keeping the keeper delay element at the end of delay time. Most notable merit is the reciprocal of the input signal to precharge-compatible dual output. Considerable number of region and consumption of power can be conserved, as a sail wide gate gives the equal function as its paired rail counterpart. The technique of conditional keeper domino (CKD) are relatively insensitive to reasonable timing variations. Thus, the conditional keeper domino (CKD) is used to achieve less power consumption and leakage tolerant [10].

C. High speed domino

High speed domino [4] has better operating speed and it is operated only under the condition of clock input in high. High speed domino consists of two transistors, they are PDN and keeper transistor. Variance in the PDN and keeper transistor make High Speed domino to operate in high speed. The disadvantage of the High-Speed domino is consuming more power and if the noise of the input is increases lead to give the output false. Thus, the High-Speed domino used in the high speed applications but it has less noise -immunity factor than other domino circuit design techniques[10].

D. Diode footed domino

In Diode Footed Domino (DFD), there is a N-MOS transistor is connected in series with the evaluation network [1]. The sub threshold leakage decreases due to the effect of stacking inside the circuit. The leakage that occurs in evaluation transistors causes some voltage drop in the circuit in evaluation phase. There is drop in voltage due to the voltage drop in gate to source is negatively evaluation transistor. This

makes the transistor in off position. It reduces sub threshold leakage, but the drop-in voltage increases the effect of body in evaluation transistors and it reduces the sub threshold leakages. The reduction in threshold voltage increases the gate-switching voltage. The voltage is two times the threshold voltage. It offers through noise immunity performance degradation process that occurs along in there. It is happening there because of decreasing evaluation current. It can be overcome by using the transistor. Sum of both evaluation network and mirrored current gives the total evaluation current. Thus, by using the diode footed domino design noise immunity performance increases with respect to sub threshold voltage function[10].

E. Leakage current replica

The CKD which is the most applicable dynamic logic consists of two keeper transistors [see B]. The conditional keeper domino (CKD) has a disadvantage that it increases the delay of inverting circuits and gates are desired to make better noise immunity of the circuit. To overcome this the alternative method is introduced by adding leakage current replica keeper and current mirror [3]. In current mirror circuit, a transistor is designed with diode configuration. The drain is connected to the gate of P-MOS transistor. The drain voltage of transistor at low level of dynamic node because of diode configuration the reduction of leakage current causes due to drain voltage of transistor goes high. It led to reduction in leakage current. Leakage current replica is a domino circuit with leakage and noise tolerant with wide gates. To reduce the contention in which keeper is controlled with current comparison. The main advantage of leakage current replica (LCR) is reduction is the power consumption. The use of Diode-footed transistor also results in reduction of leakage and increases noise immunity [10].

F. Diode partitioned domino

The proposed diode portioned domino (DPD) decreases the stray capacitance on the domino node [6]. The diode partitioned domino (DPD) divide keeper transistor along with stray capacitance, the current of the diode partitioned domino (DPD) will become reciprocal to the size of the keeper. The input noise depends upon the size of the keeper and better condition due to the fan-in. At each partition the fan in parallel to NMOS and inversely proportional to actual dynamic circuit. The circuit needs an additional keeper. A forward bias current per semiconductor width is not appropriate for a circuit. Due to huge width of the design, it makes stray capacitance. To overcome this, use proposed diode partitioned diode (DPD) an external circuit that boost the gate voltage [10].

G. Proposed domino

The capacitances of the dynamic node are huge and the speed reduced and also prevents the noise in the gate is reduced which is parallel to wide gates. The strength and condition of the domino improved by the keeper transistor's size. Decrease in speed and increase in Power-consumption because of the huge contention and this problem can be solved if the pull-down network (PDN) performs logical function which makes the keeper transistor separate from it. Thus, the pull up current phase is differentiated with leakage current of worst case. The voltage across the diode footer uses diode footed technique in other dynamic circuits. The dimension of the diode footer transistor should be smaller than other diode footed domino (DFD) circuits so that, a keeper transistor is used to make-up the lower leakage current [10]. Thus, it results on lower delay and less power consumption due to huge size of footer and mirror transistor.

4. Comparisons

The circuit was designed using HSPICE in the high performance sixteen nanometer determination technique [9][10] and in the reference to the paper using bottleneck technology. OR gate is used with 0.8v as input, where it is operated at a frequency of 1-GHz clock frequency. In this paper normalized unity noise gain comparison is taken into account so that we can able to infer the different design techniques that which consumes less power.

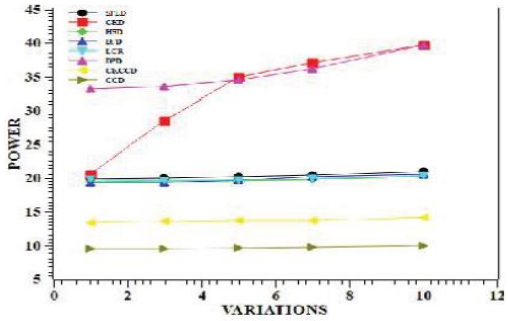

Fig. 1 Comparison of Variations on Power for 64 bit OR Gate

5. Conclusions

In this paper, various dynamic logic and static circuit design technique are reviewed based on the noise margin, power consumption, delay and high speed. Domino circuit is applied in vast variety application like dynamic memory, a microprocessor and static circuits are used in space technology. Thus, we proposed that static circuit has an advantage on withstanding in high radiation and in domino design technique the CCD takes less power and DPD requires more amount of power. HSD has the fastest domino logic design than other technique. DFD, DPD and CCD have low speed while in operation.

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